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Indium Doping Concentration Effects in the Fabrication of Zinc-Oxide Thin-Film Transistors

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ZnO semiconducting thin films were fabricated using a sol-gel method under standard atmospheric conditions and acetates as precursors. The performances of thin-film transistors (TFT) with a ZnO active channel layer and effects of indium doping on the threshold voltage of ZnO TFTs were evaluated at a low temperature (300 ℃). By examining the electrical characteristics of thin films and TFTs while doping a ZnO system with increasing indium concentrations from 0.01 to 0.1M, reductions at the threshold voltage of 5.3 V and an increase of an order of magnitude of the on/off current ratio were observed. Oxygen vacancies increase when the indium concentration increases, thus releasing electrons and increasing the channel carrier concentration. At 300 ℃, the indium-doped zinc oxide (IZO) device performance showed a mobility of 0.06 cm^2/V-s, a threshold voltage of 5.3 V, and an on/off current ratio of 10^6.

Keywords: indium zinc oxide, thin-film transistor, threshold voltage, ZnO

1. INTRODUCTION

In recent decades, the electronics industry has predominantly focused on semiconductor and display applications. The advancement of technology demands that electronic devices are light, thin, small, and bendable. Flexible electronics have potential applications as e-books, e-paper, smart cards, and solar cells. Flexible electronics involve flexibility of design, manufacturing, assembly, and use.

Flexible electronics have been manufactured since 2005 by using flexible materials as the substrate. Compared with silicon-based devices, flexible electronics offer several advantages [1-6] including low cost, low weight, flexibility, and simple modification of the surface.

Amorphous silicon thin-film transistors (a-SiTFT**)** are compatible with conventional complementary metal-oxide semiconductor (CMOS) devices. However, the low electron mobility

(<0.5 cm^2/V-s) and low-energy band gaps (e.g., 1.7 eV) of a-Si TFTs affect their speed of response and resolution for LCD applications. Flexible electronics cannot operate at process temperatures greater than 400 ℃. The current manufacture of flexible electronic devices uses organic thin films [7, 8]. Unlike metal-oxide semiconductor field-effect transistors (MOSFET), organic thin-film transistors (OTFT) use organic semiconductor materials as the semiconductor layer. Compared with CMOS transistors, OTFTs can be produced at relatively low temperatures, allowing the use of thin and inexpensive substrates. OTFT manufacture usually involves patterned evaporation [9] or spin coating [10] of organic semiconductor materials on a transistor between the source and the drain. Organic materials are more malleable and flexible than silicon is, and, thus, are appropriate for use in flexible displays.

OTFTs using pentacene as the organic channel material have been widely studied [9]; the carrier mobility and on-off ratio of these devices are not significantly different from a-Si thin-film devices. P_3HT organic semiconductor materials are fabricated using the sol-gel method, in which a solution of the precursor is spun onto the surface to deposit a thin film. Film thickness is controllable by varying the concentration of the precursor, and spin speed can be used to ensure the uniformity of the deposited film. This approach provides large-area, low-cost thin-film transistors with good performances. However, organic films exhibit low electron mobility, and the organic materials are severely affected by water and oxygen; thus, organic TFTs offer poor reliability.

Metal oxide thin films, such as In_2O_3, SnO_2, and ZnO, have been used as electrodes in flat panel displays [11, 12]. Current methods for ZnO thin-film deposition use chemical vapor deposition (CVD) or physical vapor deposition (PVD). CVD of ZnO thin films requires a high vacuum and high-temperature environment; however, flexible polyimide-based substrates cannot withstand high temperatures. PVD requires high vacuum and high voltages, but the roll-to-roll fabrication process of flexible electronics is not well suited to high vacuum environments.

Current polyimide-based flexible substrates are not reliable under ambient atmospheric conditions; however, the roll-to-roll method used in the fabrication of large-area flexible electronics is conducted at room temperature and at atmospheric pressure. An alternative ZnO film fabrication method is needed to address the issue of organic material reliability. It is possible to deposit thin films at ambient temperatures and at atmospheric pressure using sol-gel methods. Such an approach could be integrated with roll-to-roll manufacturing processes to avoid the high-temperature limitations of flexible substrates. Transparent ZnO TFTs, doped with Ga, In, or Sn, such as indium zinc oxide (IZO) [13], have been reported. The ionic radius of In^{3+} is less than that of Zn^{2+}, and thus In^{3+} ions could replace Zn^{2+} ions at substitution sites. However, there are few reports of sol-gel preparations of indium-doped ZnO TFTs.

This report describes the fabrication of ZnO semiconductor thin films under standard atmospheric conditions by using a sol-gel method and acetates as precursors. The performances of thin-film transistors (TFT) with a ZnO active channel layer and the effects of indium doping on the threshold voltage of ZnO TFTs were evaluated at a low temperature (300 ℃).

2. EXPERIMENTAL DETAILS

Fig. 1 shows the structure of ZnO and IZO-based TFTs with a 100-nm-thick SiO_2 gate dielectric fabricated on p-type silicon. The electrical performances were determined using current-voltage (I–V) analysis. The structures of the thin-film devices were examined using transmission electron microscopy (TEM, JEOL JEM-2010F) and atomic force microscopy (AFM, Veeco Dimension-5000).

The ZnO and IZO precursor solutions were prepared using zinc acetate dihydrate and indium acetate, respectively. Solutions of metal precursors were prepared in 2-methoxyethanol (**2ME**). The In:Zn molar ratio of the precursor solution varied between 1:10 and 1:1; the indium concentration ranged from 0.01 to 0.1 M, whereas the zinc concentration was maintained at 0.1 M. Metal-oxide solutions were stirred at 80 ℃ for 30 min before spin coating (Fig. 2). Fig. 3 shows the experiment flow chart. First, the p-type silicon wafer surface was treated using the RCA clean procedure to remove particles and then thermally oxidized to provide a silicon dioxide thickness of approximately 100 nm. The silicon dioxide layer was then etched using reactive ion etching (RIE), and the wafer was cleaned using standard cleaning methods to remove particles. The surface was then treated with oxygen plasma for 30 s. Semiconductor layers were spin coated onto the wafer with a ZnO or IZO solution at speeds of 500 and 1000 rpm for 30 s. Finally, the film was annealed in air at 300 ℃ for 1 h.

The gate electrode was prepared by plating the wafer backside with a 300-nm layer of Al by using thermal evaporation at 10^{-6} Torr. A shadow mask was applied to define the source and drain with a channel length and width of 70 μm and 2000 μm, respectively, followed by plating with a 300-nm layer of Al. After completion, devices were assessed using the Agilent 4156 semiconductor parameter analyzer.

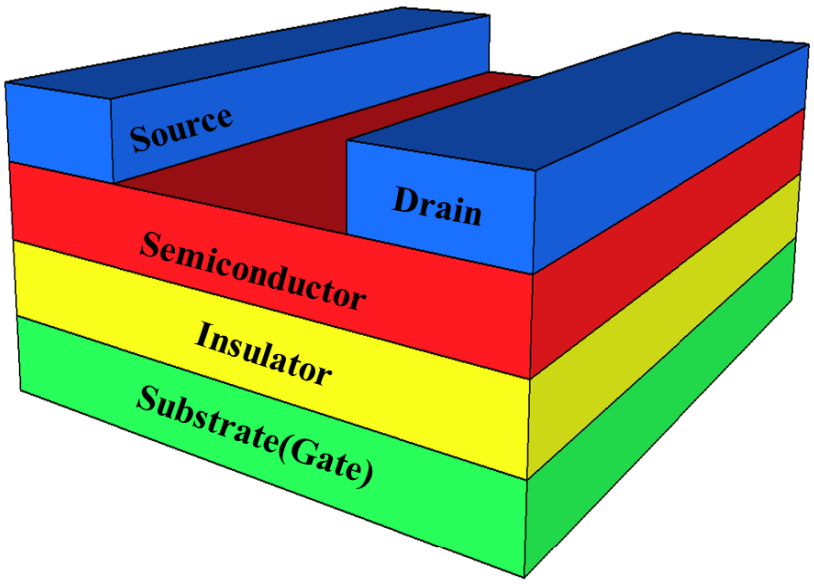

Figure 1. A schematic cross-sectional view of the ZnO and IZO structure.

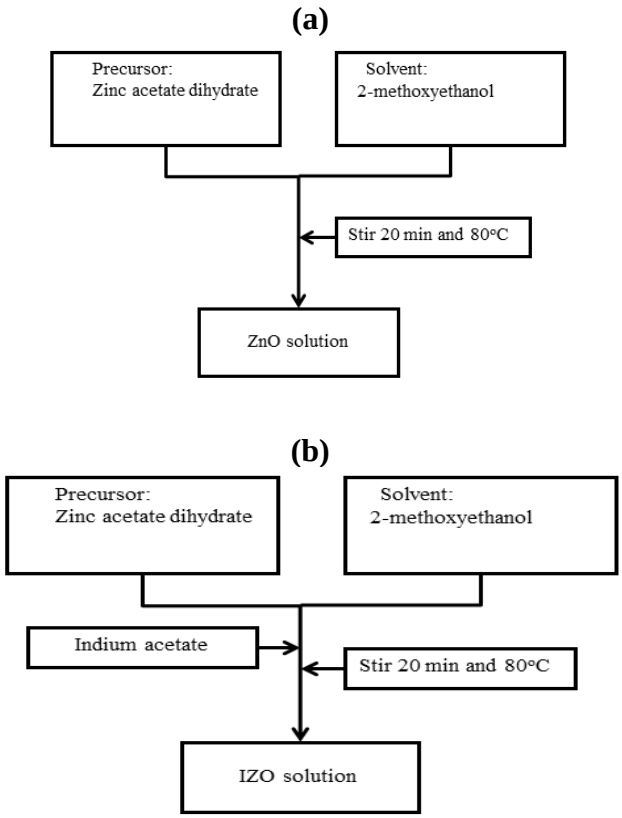

Figure 2. The sol-gel method used for the preparation of the (a) ZnO, (b) IZO solution.

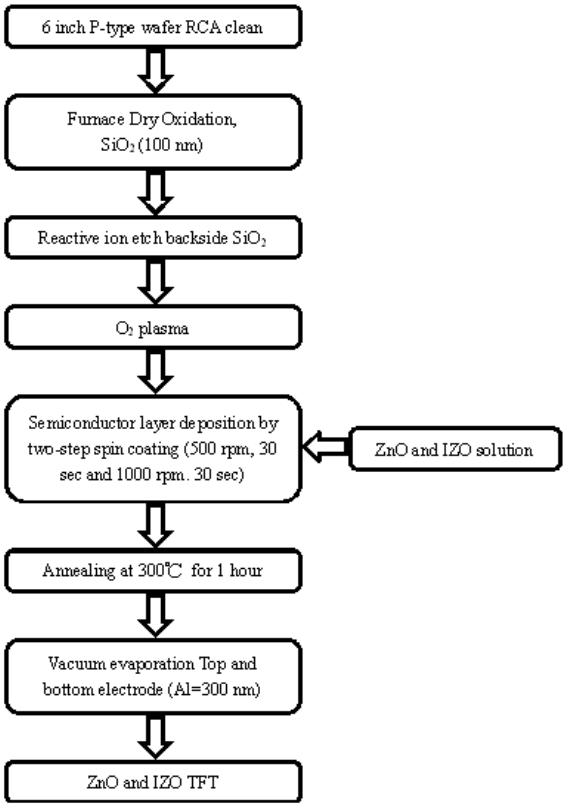

Figure 3. Outline of the ZnO and IZO TFT processing by sol-gel method.

3. RESULTS AND DISCUSSION

Fig. 4 shows the cross-sectional TEM images of the ZnO/SiO_2 structures annealed at 300 °C. The figure shows that the sol-gel method successfully deposited a smooth ZnO film at a thickness of approximately 3.7 nm. The thin-film surface morphology is crucial for operating the transistor. Fig. 5 shows a cross-sectional TEM image of the 0.01-M indium-doped IZO/SiO_2 structure annealed at 300 ℃. The TEM micrograph reveals the amorphous nature of the approximately 1.8-nm-thick IZO film, which confirms that the sol-gel method produces markedly smooth IZO thin films.

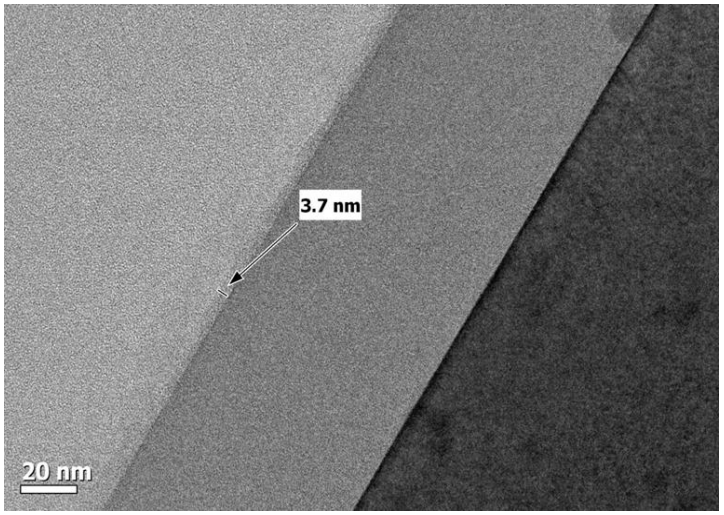

Figure 4. Cross-sectional TEM images of sol-gel-derived ZnO/SiO_2 structures annealed at 300 ℃.

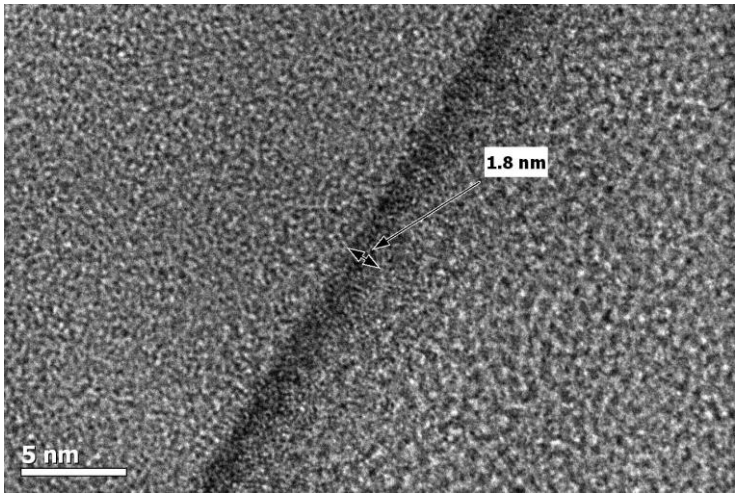

Figure 5. Cross-sectional TEM image of sol-gel-derived IZO/SiO_2 structure annealed at 300 ℃.

Fig. 6 shows the AFM images of sol-gel-derived ZnO thin films annealed at 300 ℃ for 1 h in air. The figure reveals a sample root mean square (RMS) roughness of 0.635 nm. Figs. 7 and 8 show AFM images of the indium-doped ZnO thin films. The RMS roughness values for samples with

indium dopant concentrations of 0.01 and 0.1 M are 0.552 and 0.438 nm, respectively. The surface roughness of the non-doped ZnO annealed at 300 ℃ (RMS = 0.635 nm) was substantially greater than that of the 0.01-M and 0.1-M indium-doped samples (RMS = 0.552 nm and 0.438 nm, respectively). Adding indium considerably improves the surface smoothness by decreasing the grain size [14, 15].

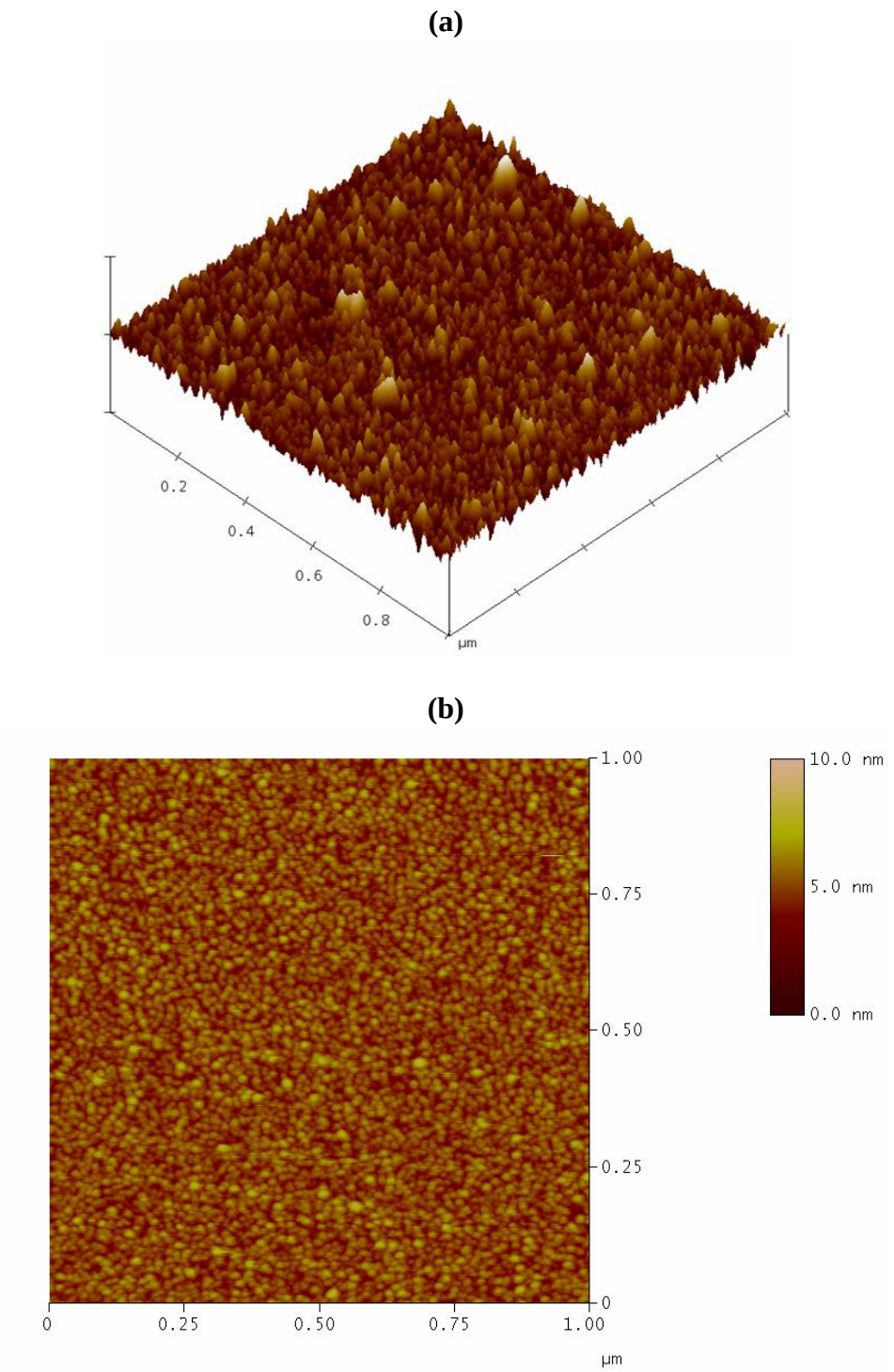

Figure 6. AFM image of the spin-coated ZnO thin film on the substrate annealed at 300 ℃, the scanning area of 1 μm^2 (a) Three-dimensional AFM image and (b) RMS roughness analysis 0.635 nm

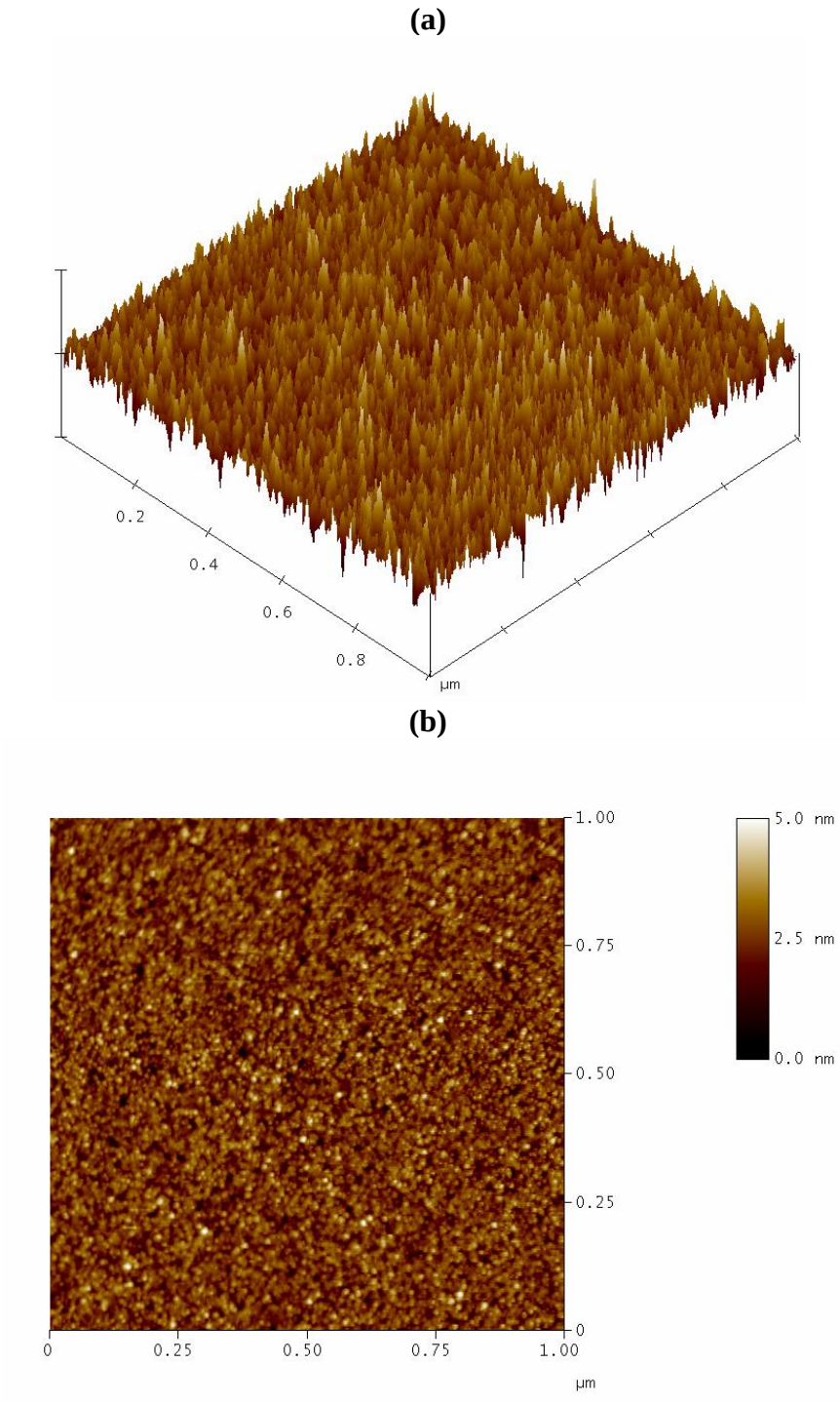

Figure 7. AFM image of the spin-coated IZO with indium concentrations of 0.01 M thin film on the substrate annealed at 300 ℃, the scanning area of 1 μm^2 (a) Three-dimensional AFM image and (b) RMS roughness analysis 0.552 nm.

Fig. 9 shows drain current-gate voltage (ID-VG) transfer characteristics at 300 ℃ for the ZnO TFT with channel lengths of 70 μm and widths of 2000 μm. The ZnO TFT produced an on/off current ratio of nearly 10^5. The on current (I_{on}) was able to sustain levels as high as 3.81×10^{-6} A at VD = 5 V,

and the off current (I_{off}) was low at 2.18×10^{-11} A, with a field-effect mobility (μFE) of 0.06 cm^2/V-s and threshold voltage (V_{th}) of 15.6 V [16].

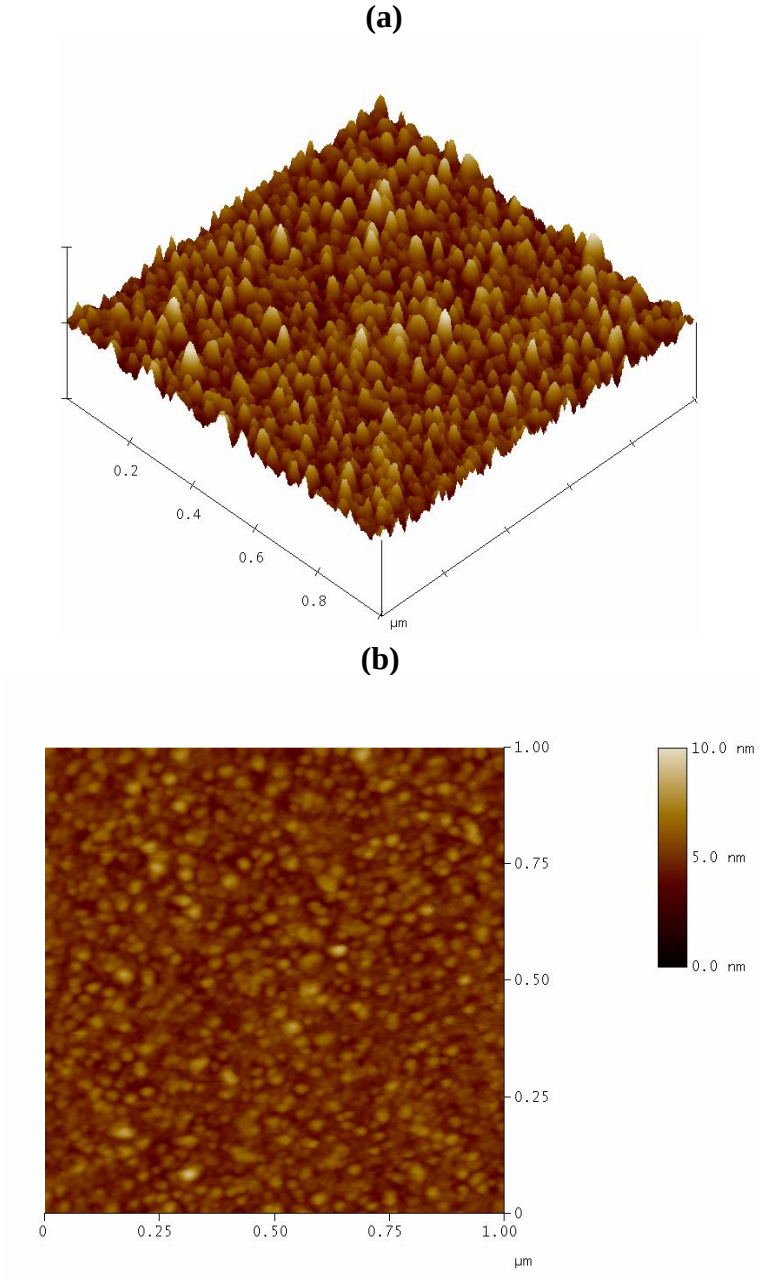

Figure 8. AFM image of the spin-coated IZO with indium concentrations of 0.1 M thin film on the substrate annealed at 300 ℃, the scanning area of 1 μm^2 (a) Three-dimensional AFM image and (b) RMS roughness analysis 0.438 nm.

A solution-processed IZO TFT with a width of 2000 μm and length of 70 μm was fabricated using spin coating IZO film and annealing at 300 °C for 1 h. Dopant concentrations were controlled at 0.01 M and 0.1 M. Fig. 10 shows the transfer characteristics of the IZO TFT with an indium concentration of 0.01 M. The I_{on} and I_{off} are 1.15×10^{-6} and 5.63×10^{-11} A, respectively. The on/off current ratio reached 10^5 for a 5-V drain to source voltage (V_{DS}). The spin-coated IZO TFTs had threshold voltages (V_{th}) of 9.31 V. Fig. 11 shows the transfer characteristics of the solution-processed

IZO TFT doped with an indium concentration of 0.1 M. The I_{on} and I_{off} were 2.24×10^{-5} and 3.52×10^{-11} A, respectively. The on/off current ratio reached 10^6, and the drain to source voltage was 5 V. The spin-coated IZO TFTs had threshold voltages of 5.3 V. Both exhibited typical n-channel behavior when operating in an enhanced mode.

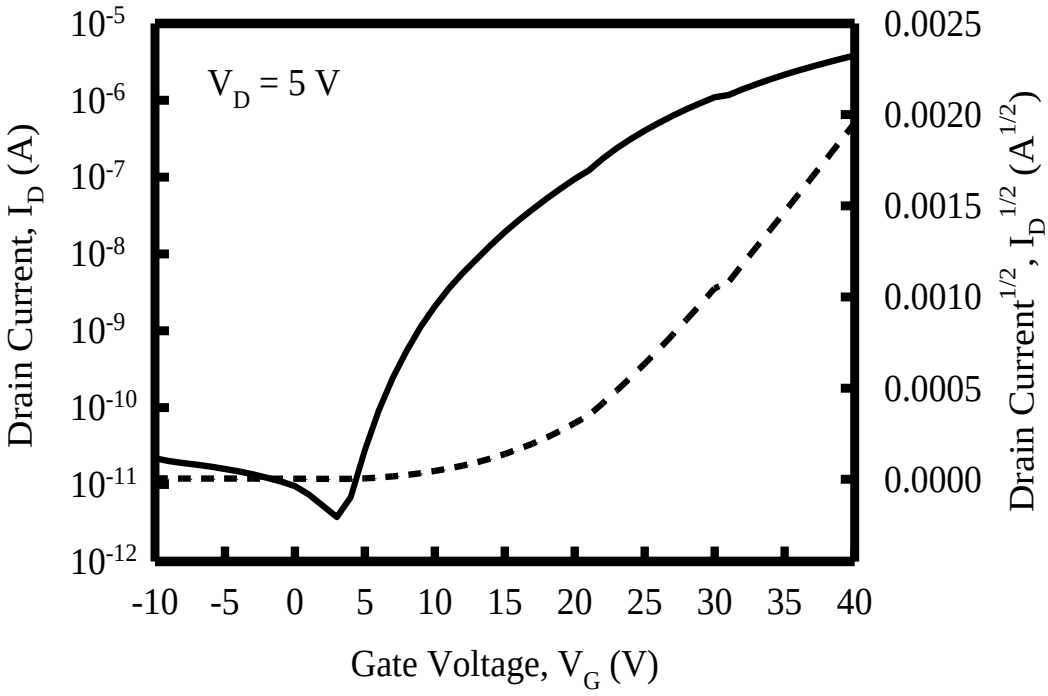

Figure 9. Transfer characteristics curves of ZnO TFT annealed at 300 ℃ by sol-gel method, VD = 5 V.

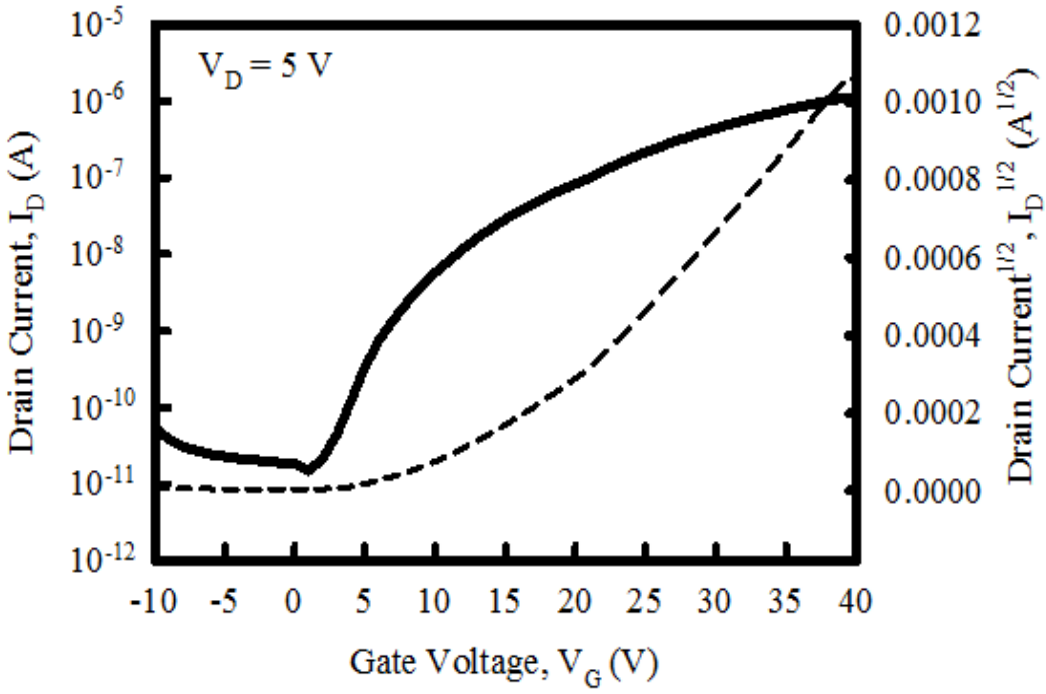

Figure 10. Transfer characteristics curves of IZO TFT with indium concentrations of 0.01 M annealed at 300 ℃ by sol-gel method, VD = 5 V.

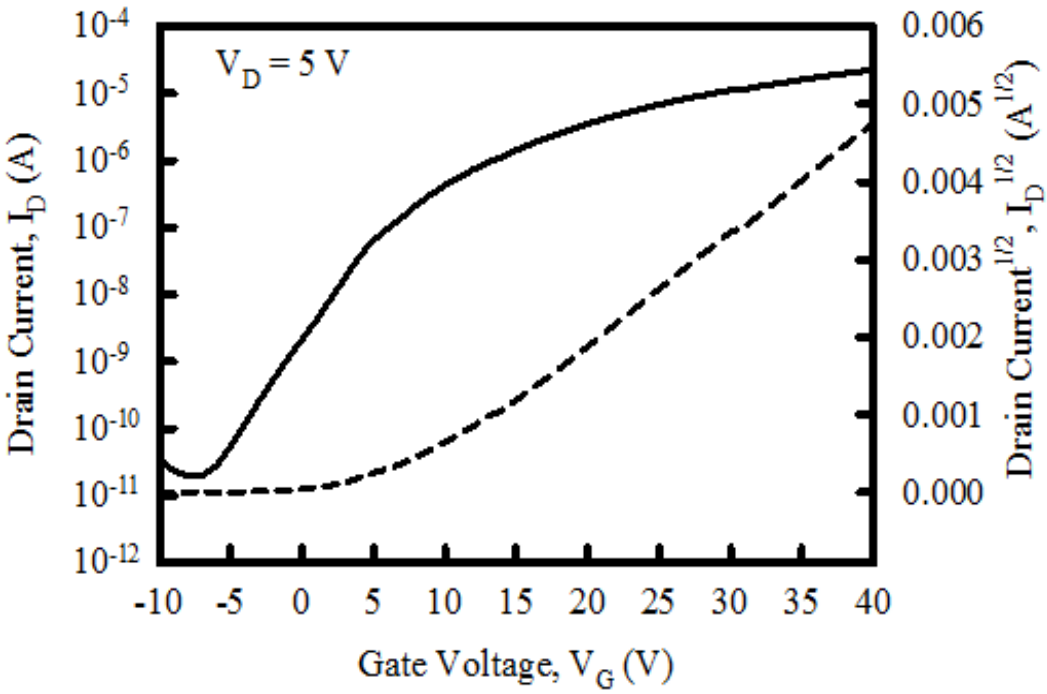

Figure 11. Transfer characteristics curves of IZO TFT with indium concentrations of 0.1 M annealed at 300 ℃ by sol-gel method, VD = 5 V.

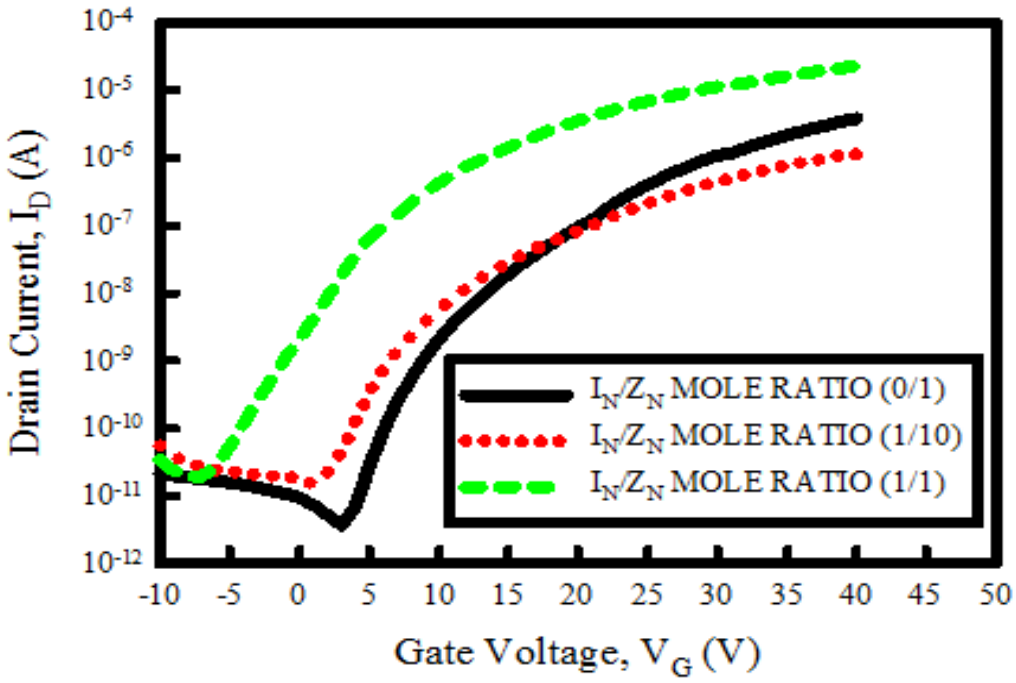

Figure 12. Transfer characteristics of TFT fabricated using ZnO channel annealed at 300 ℃ with different In/Zn Mole Ratio from 0 to 1, VD = 5 V.

Table 1. Electrical performance parameters of transistors fabricated using a ZnO channel annealed at 300 ℃ with In / Zn mole ratio.

mole ratio of In : Zn	I_{on} (A)	I_{off} (A)	$I_{on/off}$	V_{th} (V)	μ_{FE} (cm^2/V-s)
0/1(0.1M)	3.81×10^{-6}	2.18×10^{-11}	10^5	15.6	0.06
1(0.01M)/10(0.1M)	1.15×10^{-6}	5.63×10^{-11}	10^5	9.31	0.07
1(0.1M)/1(0.1M)	2.24×10^{-5}	3.52×10^{-11}	10^6	5.3	0.08

The comparison of ZnO and IZO TFTs is summarized in Table 1 and Fig. 12. The IZO TFT V_{th} value is less than that for the ZnO TFT, and the on/off current ratio was an order of magnitude greater. The decrease in threshold voltage resulted from increases in the numbers of mobile carriers. The existence of oxygen vacancies provided electrons and increased the concentration of channel carriers, leading to the reduced threshold voltage of 5.3 V (Table 1).

4. CONCLUSION

Numerous studies of semiconductors conducted at the turn of the millennium have focused on wide-band-gap compound materials. These materials are of particular interest because of their transparency in the visible spectrum and their potential for integration with both optical and electronic components. ZnO is of particular interest because it is relatively non-toxic, thermally stable, and obtained from inexpensive raw materials. This study provided high-performance solution-derived bottom-gate TFTs fabricated on a Si substrate at room temperature. Part 1 investigated the effects of annealing ZnO TFTs at 300 ℃. This paper provides a qualitative description of ZnO TFT operating principles and electrical properties. The ZnO TFT achieved a 10^5 on/off current ratio and had a large threshold voltage of 15.6 V. Thus, we studied the effects of substituting indium into the ZnO system to fabricate IZO thin films. In Part 2, the doping concentration of indium was found to influence the electrical characteristics of the IZO transistor. The addition of 0.1 M of indium optimized the transistor performance. We further demonstrated that IZO TFTs annealed at 300 ℃ exhibited superior electrical characteristics, such as a field-effect mobility of 0.06 cm^2/V-s, threshold voltage of 5.3 V, an I_{off} of 3.52×10^{-11} A, an I_{off} of 2.24×10^{-5} A, and an on/off current ratio of 10^6.

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