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# Fabrication and Characterization of Interconnected Grid-type Dye-Sensitized Solar Modules

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A process is developed for the fabrication of interconnected grid-type dye-sensitized solar cell (DSSC) module by using commercially available materials. This novel structure not only demonstrates high current output, but also exhibits high open circuit over 1 volt. In addition, the fabrication process is simple in that it allows the fabrication of a normal grid-type DSSC module with only the addition of a laser isolation treatment during substrate preparation. Finally, interconnected grid-type DSSC modules with 1.41V open circuit voltage and 5.86% conversion efficiency equal to 261.7mW power output was achieved for a low-volatility electrolyte system under a simulated 1 sun irradiation on a 12cm by 7.5 cm substrate.

**Keywords:** module; interconnected; laser scribing, solar cell;

## 1. INTRODUCTION

Dye-sensitized solar cells (DSSC) provide low cost solar electricity and perform well in niche applications under low illumination [1-4]. In the last 2 decades, efforts have focused on the synthesis of more efficient dyes [5-7], preparation of $TiO_2$ mesoporous film structures with higher diffusivity and low recombination rate [8-9], more robust and efficient electrolyte systems [10-11] and counter electrode materials with higher catalytic activity or lower cost materials [12-14]. To date, the power conversion efficiency (PCE) of DSSCs has reached 12.4% for devices containing a zinc porphyrin sensitizer and cobalt based redox electrolyte [15]. The difference in the PCE of DSSC and traditional solid-state photovoltaic systems has diminished rapidly.

A general small DSSC comprises:

(1) A dye-sensitized meso-porous $TiO_2$ photo-anode,

(2) A cathode, containing catalytic materials for $I_3^-$ reduction,

(3) An $I^-/I_3^-$ redox couple in a proper transport medium, as the electrolyte,

(4) Proper sealing material to encapsulate these components in a small chamber.

To produce a highly efficient and durable DSSC, an appropriate combination of these four components must be chosen. However, to achieve the same goal for a DSSC module of large area, additional structures, such as metal grid lines, must be used and local isolation of the transparent conducting oxide and a layer to protect against corrosive redox couples are also important. Several structures have been proposed for DSSC modules, including structures with a series connection, such as W-type [16], Z-type [17] and monolithic [18] connections, or current-collection type single cells with a large area (parallel connection) [19-20]. In general, series connected modules have a high voltage but low current output, while parallel connected modules have a low voltage and high current output.

DSSCs are known to outperform silicon solar cells under weak or fluorescent light and their PCE is less sensitive to the angle of the incident light [4]. They are also more flexible in terms of shape and more versatile in terms of color. These advantages make DSSCs ideal for consumer electronics integration. For series connected type modules, the open circuit voltage ($V_{OC}$) is proportional to the number of $TiO_2$ strips; this feature can limit the variety of applications and complicate the design of the electrical circuitry. To avoid these drawbacks and retain a simple fabrication process, grid-type DSSC modules are more suitable for integration in portable devices than series connected types.

However, grid-type modules are not perfect either; they usually suffer from a significant loss of fill factor, especially when the panel size increases, because of the very large photocurrent [21]. The voltage of conventional grid-type DSSC modules (0.5 to 0.7 volt) is too low to drive any functional IC or to store in battery. A commercial voltage-transformer IC also experiences significant energy loss at this voltage level. Therefore, there is a dilemma in choosing the type of module used for portable devices.

This study develops a process to fabricate a “hybrid” module structure, which uses two identical grid-type sub-modules on a single FTO glass substrate. These are interconnected, in order to increase the output voltage. This structure provides an open circuit voltage that is double that of a conventional grid-type module, so that a commercial voltage-transformer IC can be easily used to accommodate the voltage requirements of a portable device.

## 2. EXPERIMENTAL

The process flow for the production of an interconnected grid-type DSSC module is detailed in Figures 1, 2 and 3; these show the photo-electrode process, the nano-Pt counter electrode process and the fabrication process, respectively. For clarity, these three processes are separately described in the following sections.

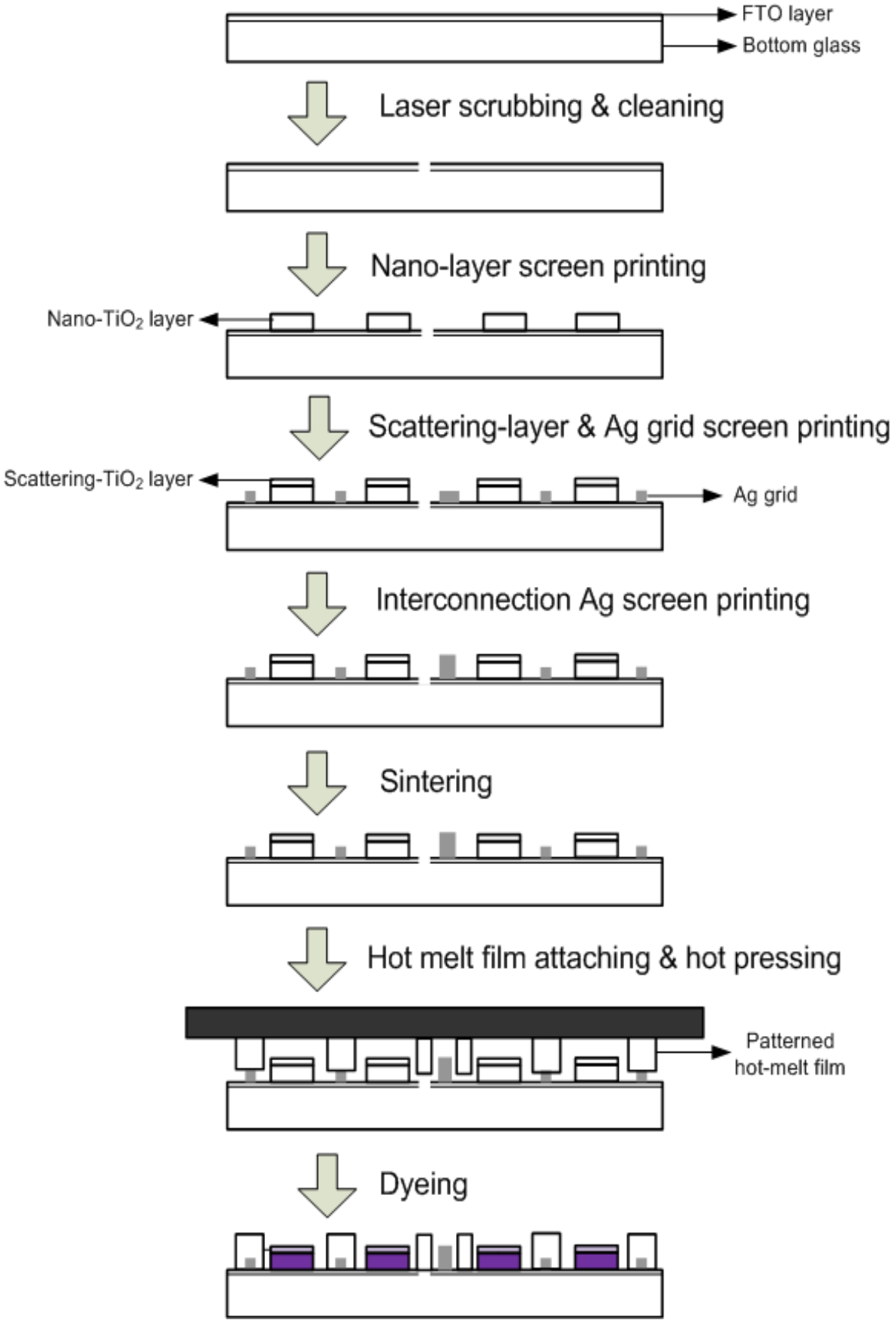



**Figure 1.** Schematic drawing of the process to produce the anode for an interconnected grid-type DSSC module

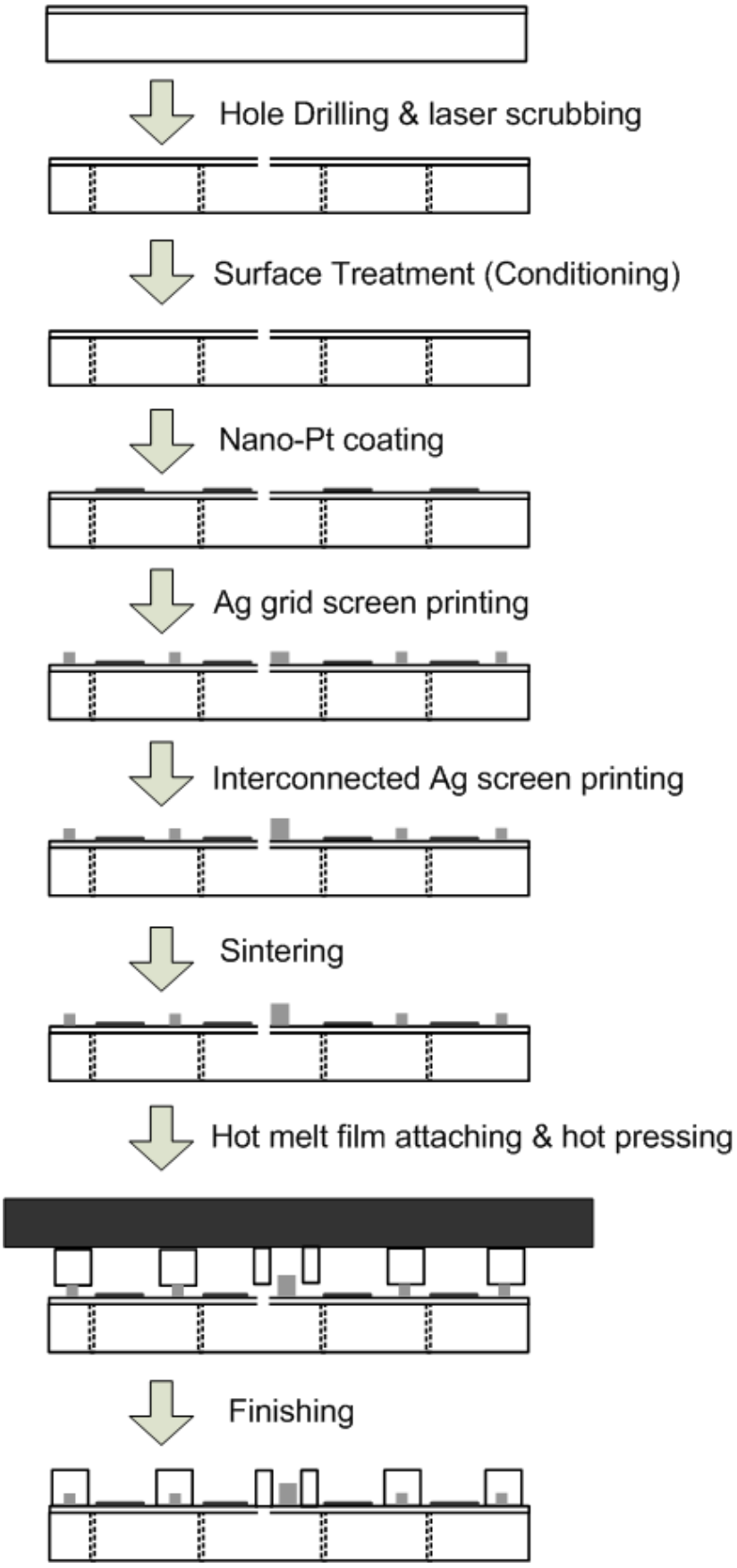



**Figure 2.** Schematic drawing of the process to manufacture the counter electrode for an interconnected grid-type DSSC module

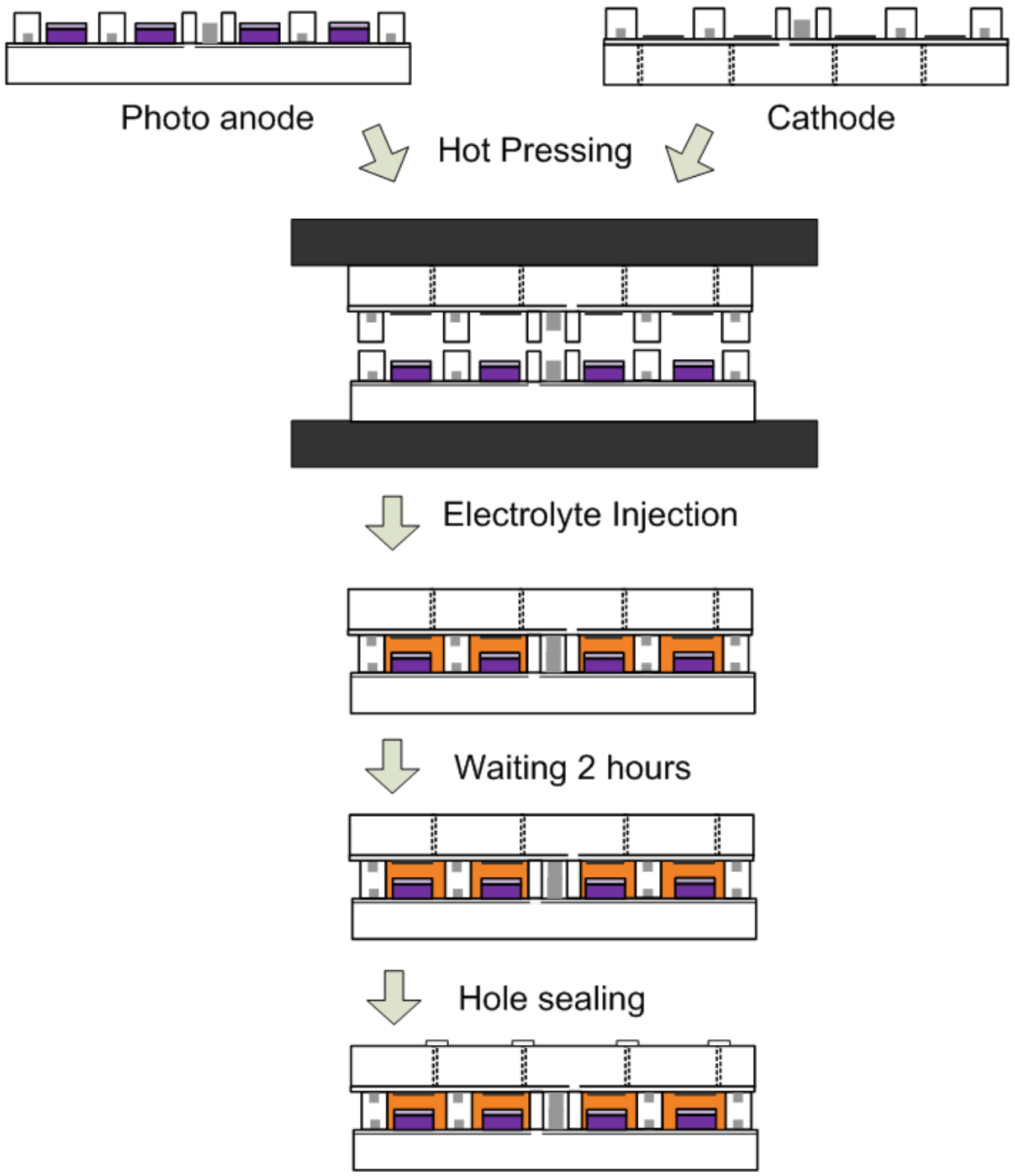



**Figure 3.** Schematic drawing of the assembly process for an interconnected grid-type DSSC module

*2.1 Preparation of the photo-electrode:*

Firstly, a Nd:YAG laser (10W, 30kHz) is used to scribe out the FTO layer in the center region of a piece of FTO substrate (12cm x 7.5cm, NSG, 3.1mm, 9$\Omega sq^{-1}$), before it is cleaned in a commercial glass cleaner bath (5%, PK-LCG545) for 10 minutes and then dried in a hot air chamber. Then a bi-layer $TiO_2$ film with a Ag grid pattern is sequentially screen printed onto the FTO glass, using $TiO_2$ paste (PNT series, Tripod, Taiwan; average particle size=18-20nm) as an active layer, commercial

scattering $TiO_2$ paste (JGC&C PST400C, Japan) as a light scattering layer and commercial silver paste (EPI Technology, Taiwan, PTG series) as a current collector. It is worth noting that the Ag line in the center region of the substrate is screen printed twice, so that it forms a raised plane that touches another Ag line on the counter electrode, which connects the left side and right sides of the substrate. After the bi-layer $TiO_2$ film and the Ag grid are printed on the FTO glass, the substrate is sequentially sintered at 325$^o$C for 30 minutes, 375$^o$C for 30 minutes, 450$^o$C for 30 minutes and 500$^o$C for 30 minutes, using a programmable oven with atmospheric control. After sintering and cooling of the substrate to ambient temperature, a pre-pouched hot-melt film (Surlyn 1706, 30μm), matching the designed pattern is attached to the substrate. These are then passed into a programmable hydraulic hot-presser for 3 minutes at 100$^o$C in a vacuum, until the hot-melt film fully covers the Ag pattern, except for the Ag line in the center region, which remains uncovered. Finally, dye impregnation is achieved by immersing the prepared $TiO_2$ electrode in a 0.4mM N719 ethanol solution in a programmable dyeing tank, maintained at 40$^o$C for 5 hours, to complete the preparation of the photo-anode.

### *2.2 Nano-Pt counter electrode*

Before making the counter electrode, injection holes are pre-drilled and the center region of the FTO layer is also laser-scribed. The nano-sized Pt counter electrode is prepared using a published "2-step dip coating process" [13, 22-24] as follows: the Ag pattern is first screen-printed and sintered at 500$^o$C for 30minutes on the FTO glass (NSG, 3.1mm, 9Ωsq$^{-1}$). The pre-punched hot-melt film is then attached and hot-pressed onto the substrate, to protect the Ag pattern; note that the central Ag line is also exposed for interconnection. When the remaining Ag pattern is well protected by the Surlyn, it is rinsed in an aqueous bath containing commercial TCO cleaner (2% of PK-LCG545) and then immersed into a solution containing 4% conditioner (ML371, Rockwood) for 5minutes at 60$^o$C. This treatment changes the surface charge state of the FTO surface to facilitate nano-particle adsorption. The conditioned substrate is then immersed into nano-Pt ink to adsorb nano-Pt and complete the preparation of the counter electrode.

### *2.3 Module Fabrication*

The photo-electrode and counter electrode are laminated by placing them face to face in a hydraulic hot-press in a vacuum chamber, at 110$^o$C for 4 minutes. It is observed that the boundary of the 2 hot-melt films disappears, indicating that the lamination process is complete. The module is then removed from the hot-press and cooled to ambient temperature in a second press. An electrolyte containing 1.2M PMII (1-methyl-3-propylimidazolium iodide), 0.5M NMB(N-methyl-benzimidazole), 0.15M $I_2$ and 0.1M GuSCN (Guanidinium thiocyanate) in γBL/EMITCB(γ-butyrolactone/1-ethyl-3-methylimidazolium tetracyanoborate, 3:1 in volume ratio is injected into the chamber formed by the hot-melt films, via a pre-drilled hole on the counter electrode side, using a self-designed electrolyte injector. Finally, the injection holes are hot sealed using a piece of thin cover glass with a hot-melt film underneath as an adhesive.

*2.4 Module characterization:*

The photocurrent-voltage (I-V) curve of the DSSC module was measured using a computer-controlled digital source meter (Keithley 2400), under simulated AM1.5, 1 sun irradiation (YAMASHITA DENSO YSS-150A). In addition to the standard full sun condition, neutral density filters (ND50, ND10, ND5; Shibuya Optics) were used to measure the performance of these modules under simulated conditions of low light.

## 3. RESULTS AND DISCUSSION

*3.1 Laser scribing of FTO layer*

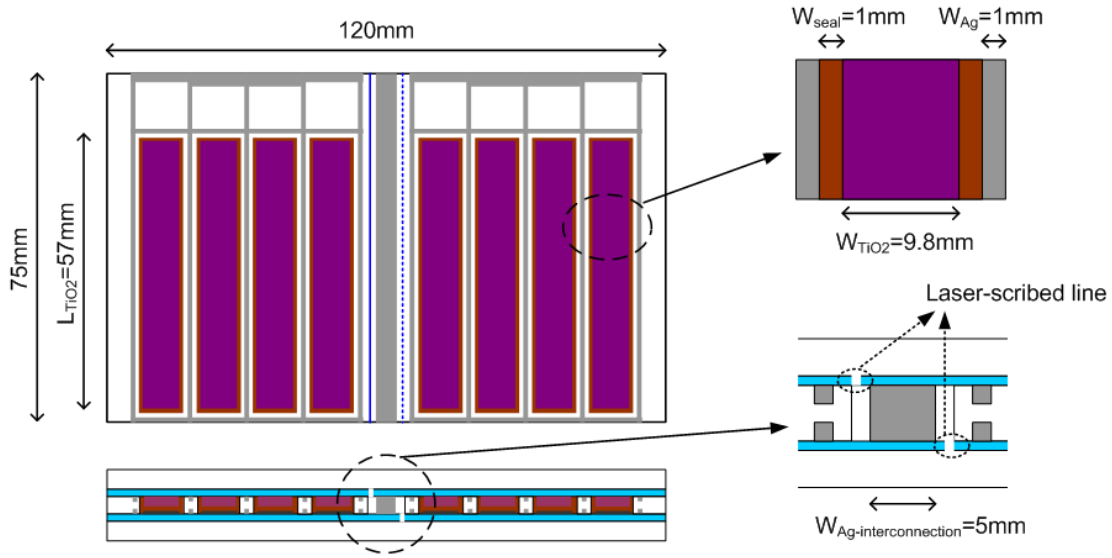



**Figure 4.** Schematic drawing of interconnected grid-type DSSC modules, where $L_{TiO2}$= length of the $TiO_2$ strip, $W_{TiO2}$=width of the $TiO_2$ strip, $W_{Ag}$= width of the Ag grid line and $W_{Seal}$=width of the seal structure

The design of the grid-type DSSC module is detailed in Figure 4. From Figure 4, it is easily seen that this interconnected grid-type module is, in fact, composed of 2 identical pieces of conventional grid-type module with an interconnecting configuration in the junction region of the two modules. This interconnecting configuration is similar to that in the structure of a conventional Z-type module [17]. This kind of module combining parallel-connected and series-connected structure in a single device is seldom reported and elaborated [24]. It is vital to ensure accurate location of the isolation, in order to ensure that both sides are properly connected in series; therefore the effect of laser scribing the FTO layer is first examined.

Figure 5a shows the scanning electron microscope (SEM) cross-sectional image of the FTO glass used in this study. From Figure 5a, it is seen that thickness of the FTO layer is approximately

500-600nm. Since the FTO layer is the only material that makes the substrate electrically conductive, it must be removed completely, to ensure electrical isolation

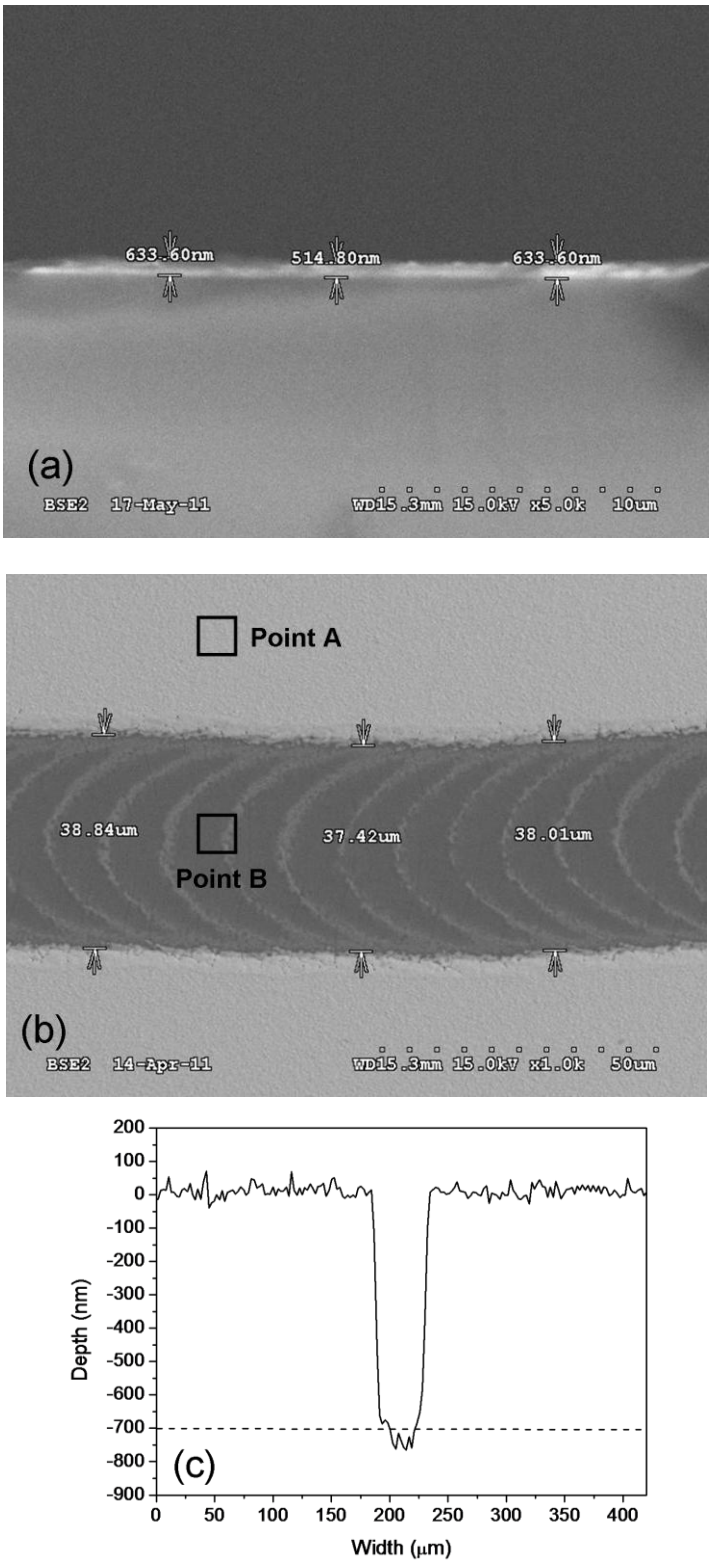



**Figure 5a.** Cross-sectional image of the FTO glass used in this study; 5b: top-view image of the laser-scribed line, showing that the line width is approximately 38μm on average; 5c: depth profile of the laser-scribed line in Figure 5b.

The SEM top-view image and the corresponding depth profile of the scribed line are shown in Figure 5b and Figure 5c, respectively. It is seen that the width of the scrubbing line is approximately 38μm and the depth is approximately 700 nm. An elemental composition analysis was also performed on the FTO surface (point A in Figure 5b) and the valley of the scribed line (point B in Figure 5b) and this is summarized in Table 1. As shown in Table 1, the major elements at point A are tin and oxygen and their atomic ratio is just slightly less than 1:2, due to fluorine doping. In contrast, there is no tin signal at point B, but silicon (20.82%) and sodium (7.02%) are present, which means that the FTO layer has been totally scribed by the laser beam and so the bottom of the sodium glass is exposed. The electrical isolation of the scribed line is also confirmed to be more than 20MΩ, using an ohmmeter.

**Table 1.** EDX/AES analysis of FTO glass and laser scrubbed region as indicated on Figure 5b.

| Element | FTO layer (Point A) | | Scribed line (Point B) | |
|---|---|---|---|---|
| % | Weight | Atom | Weight | Atom |
| C | 1.11 | 4.23 | 0 | 0 |
| O | 23.32 | 66.65 | 60.72 | 72.14 |
| Na | 0 | 0 | 8.49 | 7.02 |
| Si | 0 | 0 | 30.79 | 20.84 |
| Sn | 75.57 | 29.12 | 0 | 0 |

*3.2 The Performance of the Interconnected Grid-type DSSC Module*

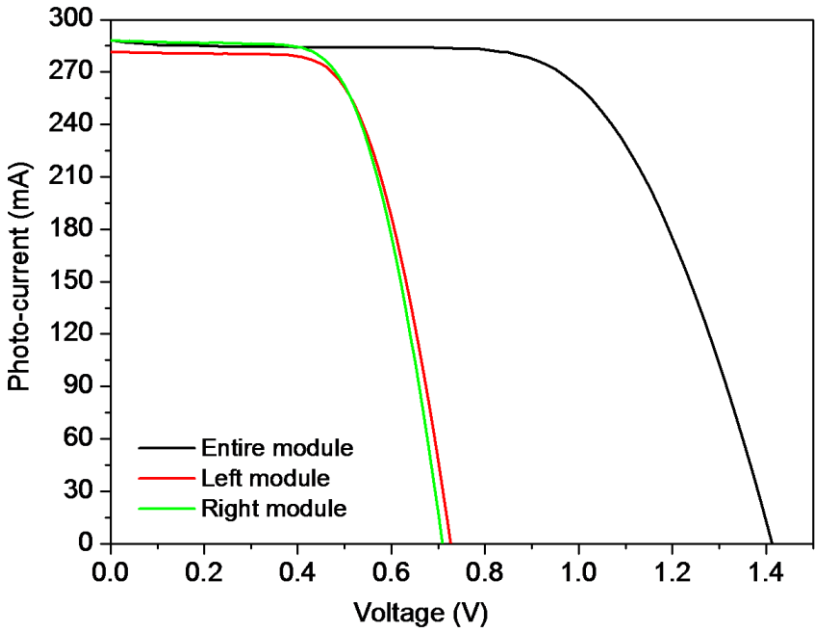
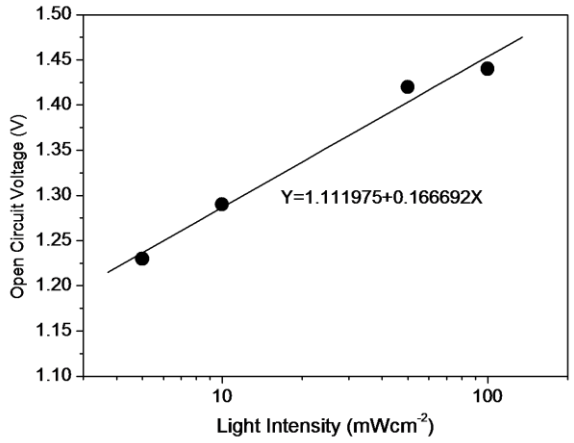



**Figure 6.** I-V curves for the interconnected grid-type DSSC module.

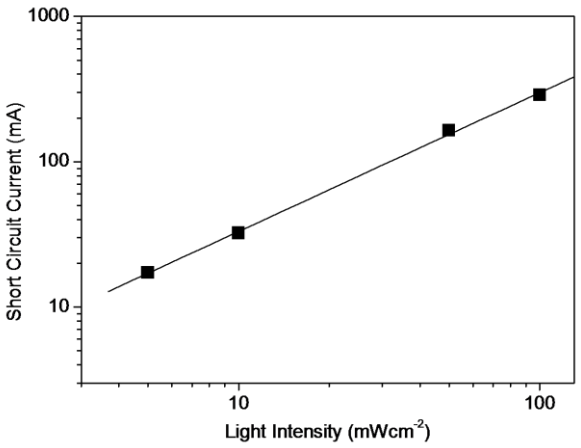
Figure 6 shows the I-V curves of the interconnected grid-type DSSC modules and the corresponding I-V parameters are summarized in Table 2. For comparison, the individual I-V curve of each grid-type module is also measured by masking either the left or the right part of the module, using a piece of black plastic. From Table 2, it is seen that the open circuit voltage ($V_{OC}$) of the entire module is 1.41V, the short circuit current ($I_{SC}$) is 287.7mA, the fill factor (FF) is 0.64 and the power conversion efficiency (PCE) reaches 5.86%. Compared with the I-V parameters for the two individual grid-type modules, the $V_{OC}$ of whole module is very close to the sum of that of the two individual grid-type modules (1.44V), while the $I_{SC}$ of the whole, the left side and the right side module remain at almost the same value of 280mA, which indicates that the fabrication process is stable and reproducible.

**Table 2.** I-V parameters of left side, right side grid-type module and entire interconnected module

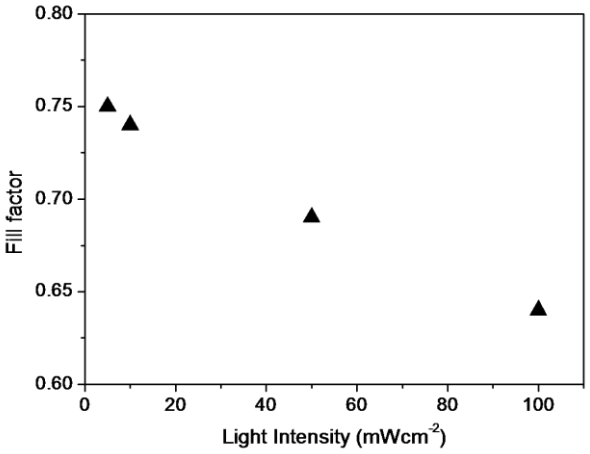
| | $V_{OC}$(V) | $I_{SC}$ (mA) | FF | PCE (%) | $P_{Max}$ (mW) |
|---|---|---|---|---|---|
| Entire module | 1.41 | 287.7 | 0.64 | 5.86 | 261.7 |
| Left module | 0.73 | 281.5 | 0.64 | 5.87 | 131.0 |
| Right module | 0.71 | 288.1 | 0.64 | 5.87 | 131.2 |




A




B




C

**Figure 7.** (a) Dependence of $V_{OC}$ on light intensity, (b) $I_{SC}$ versus light intensity and (c) FF versus light intensity of whole module.

This result also shows that the series-connected structure functions very well and, therefore, the loss of efficiency is negligible.

The photovoltaic performance of the interconnected grid type module under various light intensities is summarized in Table 3. Figure 7(a) shows the dependence of $V_{OC}$ of the entire module on light intensity. The slope of the plot of $V_{OC}$ versus light intensity is approximately 83mV on average, for a single grid-type module , which corresponds to an ideality factor, n=1.41. This result suggests that surface-trapping states participate in the charge recombination reaction. In other words, the fabrication process could be further improved, especially the surface treatment, wherein the blocking layer [26] that is applied to the FTO glass, prior to $TiO_2$ printing, is absent from the current process.

**Table 3.** IV parameters of the interconnected grid-type DSSC module under various light intensities.

| Light Intensity ($mWcm^{-2}$) | $V_{OC}$(V) | $I_{SC}$(mA) | FF | PCE (%) | $P_{Max}$ (mW) |
|---|---|---|---|---|---|
| 100 | 1.41 | 287.7 | 0.64 | 5.86 | 261.7 |
| 50 | 1.42 | 163.7 | 0.69 | 7.18 | 160.0 |
| 10 | 1.29 | 32.2 | 0.74 | 6.91 | 30.9 |
| 5 | 1.23 | 17.2 | 0.75 | 7.14 | 16.0 |

Figure 7(b) shows the plot of $I_{SC}$ versus light intensity; it is worthy of note that the $I_{SC}$ tends to deviate from linearity at high light intensities. This is due to insufficient mass transportation in the GBL/EMITCB-based electrolyte system. The relationship between fill factor and light intensity, shown in figure 7(c), indicates that FF decreases as light intensity increases. This is attributable to the series resistive loss associated with the large active area of $TiO_2$ (22.34 $cm^2$ in each module) [27].

*3.3 The Reliability of the Interconnected Structure:*

To further determine the reliability of the interconnected structure, an external wire pack was connected between the two grid-type modules, to observe the difference between internal and external series connection. If the vertical contact of the interconnected structure is imperfect, there is a noticeable difference to the I-V curve, when an external connection is made, during I-V measurement. Table 4 lists the I-V parameters of the interconnected grid-type module, measured using internal and external connections. It is seen from Table 4 that the variation in the measurement methods between that using the existing interconnection and that using external series wiring is basically negligible.

**Table 4.** Comparison of IV characteristics, measured using as-prepared interconnection and external connection

| Measuring Method | $V_{OC}$(V) | $I_{SC}$ (mA) | FF | PCE (%) | $P_{Max}$ (mW) |
|---|---|---|---|---|---|
| Interconnection<br>(% of external connection) | 1.41<br>(98%) | 287.7<br>(>99%) | 0.64<br>(102%) | 5.86<br>(99%) | 261.7<br>(99%) |
| External Connection<br>(auxiliary wiring) | 1.44 | 288.6 | 0.63 | 5.92 | 264.4 |

It was previously reported [28] that an imperfect interconnection structure causes the overall module to have either a low shunt resistance or a significantly increased series resistance; both of these effects produce a low FF and hence cause a reduction in the overall PCE. The results show that this novel hybrid module structure demonstrates good electrical isolation and sound vertical electrical connection in the right position, so the FF can remain very stable for all test conditions (left, right, internal and external). In standard series connected module structures such as monolithic, Z-type and W-type interconnected module structures, the number of interconnection elements is proportional to the number of $TiO_2$ strips, so it is difficult to simultaneously maintain good interconnection and maximize the $TiO_2$ area. However, because of the limited number of interconnection elements required by this structure (only one in this case), it is easy to provide more $TiO_2$ area in the grid-type module region. Consequently, the entire substrate area can be used, without sacrificing photovoltaic performance.

## 4. CONCLUSIONS

A new type of DSSC module structure, which uses a combination of grid-type structure and Z-type structure was fabricated and characterized. This structure has several advantages, such as high $V_{OC}$, which allows efficient IC integration, high aperture ratio, which allows better utilization of the substrate, and a limited number of interconnection elements, which simplifies the fabrication process and quality control. It is also seen that this type of module provides good performance in low light environments (PCE>7%), which allows potential applications in indoor environments. Future studies might involve tuning the fabrication process by coating a thin blocking layer onto the substrate, in order to further improve the photovoltaic performance.

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