Int. J. Electrochem. Sci., 10 (**2015**) 6500 - 6508

International Journal of
ELECTROCHEMICAL
SCIENCE
www.electrochemsci.org

Low-Temperature Formed Quaternary NiZrSiGe Nanocrystal Memory

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Received: 6 May 2015 / *Accepted:* 29 May 2015 / *Published:* 24 June 2015

This study investigated the formation of quaternary NiZrSiGe nanocrystal (NC) flash memory by using the sol-gel spin-coating method. A solution of nickel dichloride, zirconium tetrachloride, silicon tetrachloride, and germanium tetrachloride was used as a precursor to form the sol-gel thin film. Unlike the NiZrSi control sample that exhibited a continuous and smooth film after anneal, the NiZrSiGe transformed into NCs after undergoing thermal annealing in an O_2 ambient. Based on TEM analysis, the size of the nanocrystals was 2-4 nm. Compare to the NiZrSi control sample, the NiZrSiGe memory exhibits improved electrical performance in memory windows, program/erase speed, and device reliability. The memory window of the quaternary NiZrSiGe nanocrystal memory was approximately 3.84 V. The retention characteristics of the memory can be up to 10^6 s at room temperature measurement with an approximately 8% charge loss, or an approximately 10% charge loss at 85 °C measurement. The V_t shift of the program and erase states after 10^4 cycles was approximately 1 V. These results show that quaternary NiZrSiGe nanocrystal devices exhibit excellent memory performance.

Keywords: SONOS, flash memory, nanocrystal, non-volatile

1. INTRODUCTION

Flash memory devices have generated increasing interest in many electronic products because of their robust reliability, inexpensive, and low power consumption features [1-3]. A poly-silicon floating gate is adopted for the customary flash memory to store charges in a floating gate (FG). However, as the feature size shrink to nano size, a charge loss problem of the floating gate becomes

more severe [4]. Stored charges leak because repeated program and erase cycles form defects in the tunneling oxide [5]. Therefore, discrete trap memory devices, such as thin film poly-Si-oxide-nitride-oxide-silicon (SONOS) or nanocrystal (NC)-based memories, have been widely studied to replace the aforementioned FG in memory applications [6-8]. This NC memory is expected to preserve trapped charges more efficiently because of the discrete charge storage node, while still demonstrating excellent features such as fast program and erase speeds, low programming potentials, and high endurance. Hence, this type of memory can significantly enhance device reliability [9].

Researchers have reported many methods of fabricating nanocrystals, including atomic layer deposition [10], physical vapor deposition [11], and chemical vapor deposition [12]. King fabricated Ge NCs by oxidizing an ion-implanted $Si_{1-x}Ge_x$ layer, thus achieving quasi-nonvolatile memory operation with a 0.4 V threshold-voltage shift [13]. Choi formed titanium nitride (TiN) NCs with an aluminum oxide (Al_2O_3) gate dielectric using the co-sputtering method [14]. Gerardi et al. used low-pressure chemical vapor deposition (CVD) to fabricate Si NCs with a density of up to 2×10^{12} cm^{-2} [15]. Hu formed cobalt-silicide NCs by annealing Ge-doped cobalt-silicon thin film in an O_2 ambient [16].

In contrast to previous methods, a relatively simple and inexpensive technique is presented in this paper for forming NCs [17]. We fabricated a sol-gel film by using spin coating method, and the film transformed into a metal-oxide NCs after undergoing thermal annealing in an O_2 ambient. The hydrolysis, condensation, and polymerization steps in this sol–gel process form metal oxide networks [18]. These reactions play significant roles in modifying the properties of the final material. The most crucial feature of sol-gel processing is its ability to synthesize various types of materials, known as “inorganic-organic hybrids” [19, 20]. Film preparation based on spin coating is much simpler than other methods because of its simplicity in process, low-cost, and lower tool price. In addition, film fabricated by this method can be operated in normal environment without any expensive vacuum system that other methods used. [21, 22].

Although many sol-gel derived materials have been applied in flash memory, few multi-composited materials such as quaternary metallic oxide materials are studied. In this paper, the quaternary NiZrSiGe NCs were formed by using the sol-gel spin coating method. These NCs were used as a charge trapping material in flash memory. In addition, the ternary NiZrSi film was also fabricated as the compare sample. The properties of the memory window, program and erase speeds, retention, endurance, and gate and drain disturbances are assessed to evaluate the performance of the multi-composited NiZrSiGe NCs devices.

2. MATERIALS AND METHODS

The fabrication of the NC memory began with the local oxidation of silicon (LOCOS) isolation on a 6-in, p-type (100) silicon wafer. A tunnel oxide layer measuring 10 nm thick was thermally grown at 925 °C by performing furnace oxidation. The charge trapping material was prepared using a sol-gel spin coating method. The precursors used for the preparation of the sol-gel solution were analytical reagent grade nickel dichloride ($NiCl_2$-$6H_2O$, 99.5%, Aldrich), zirconium tetrachloride ($ZrCl_4$, 99.5%, Aldrich), silicon tetrachloride ($SiCl_4$, 99.5%, Aldrich), and germanium tetrachloride ($GeCl_4$, 99.5%,

Aldrich). Here we dissolved and mixed all these precursors together by using Ethanol (EtOH) as the solvent. To obtain smaller particles, a drop of hydrochloric (HCl) acid was added to the samples and stirred for 30 min when preparation. The sol-gel solution had a 1:1:1:1:1000 molar ratio of $NiCl_2$-$6H_2O$: $ZrCl_4$: $SiCl_4$: $GeCl_4$: EtOH for fabricating NiZrSiGe film. The control sample, NiZrSi film, used 1:1:1:1000 molar ratio of $NiCl_2$-$6H_2O$: $ZrCl_4$: $SiCl_4$: EtOH. We dropped the solutions on silicon oxide substrates and then spin-coated for 60s, 3000 rpm at room temperature. After undergoing rapid thermal annealing (RTA) at 900 °C for 60 s in an O_2 ambient, the coated sol-gel thin film was transferred into NCs. A 20-nm thin oxide film, named blocking oxide, was then deposited using plasma-enhanced CVD tetraethoxysilane oxide. Before the deposition of the 200-nm amorphous Si gate electrode, the blocking oxide was densified by annealing in an N_2 ambient at 900 °C for 30 s to diminish the defects. Finally, gate pattering by performing plasma etching, source/drain (S/D) formation, and the remaining MOS processes were applied to complete the device. Fig. 1 shows a schematic diagram of the NC memory device structure.

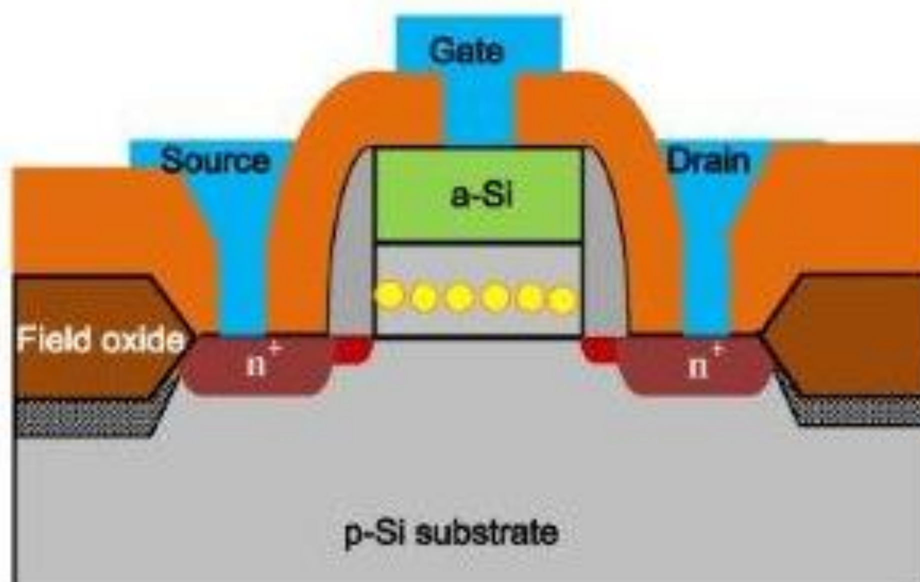

Figure 1. Schematic diagram of the quaternary NiZrSiGe NC memory structure.

The microstructures of the quaternary NiZrSiGe NCs were examined using transmission electron microscopy (TEM). The electrical characteristics of the quaternary NiZrSiGe NC memories were determined using a Agilent4156 semiconductor parameter analyzer. The feather sizes of the devices reported in this paper had a channel width and length of 10 μm and 0.35 μm, respectively.

3. RESULTS AND DISCUSSION

Figs. 2(a) and (b) show cross-sectional transmission electron microscope images of NiZrSiGe and NiZrSi, respectively, for samples annealed at 900 °C for 60 s. It is clearly seen that NiZrSiGe

sample show discrete NCs, whereas the NiZrSi sample remains continuous. The average crystal size of NiZrSiGe NCs is approximately 2-4 nm in diameter (as shown in the inset). Both samples show visible lattice fringes in pictures, which clearly denote crystallization into well-ordered nano-structured features [23].

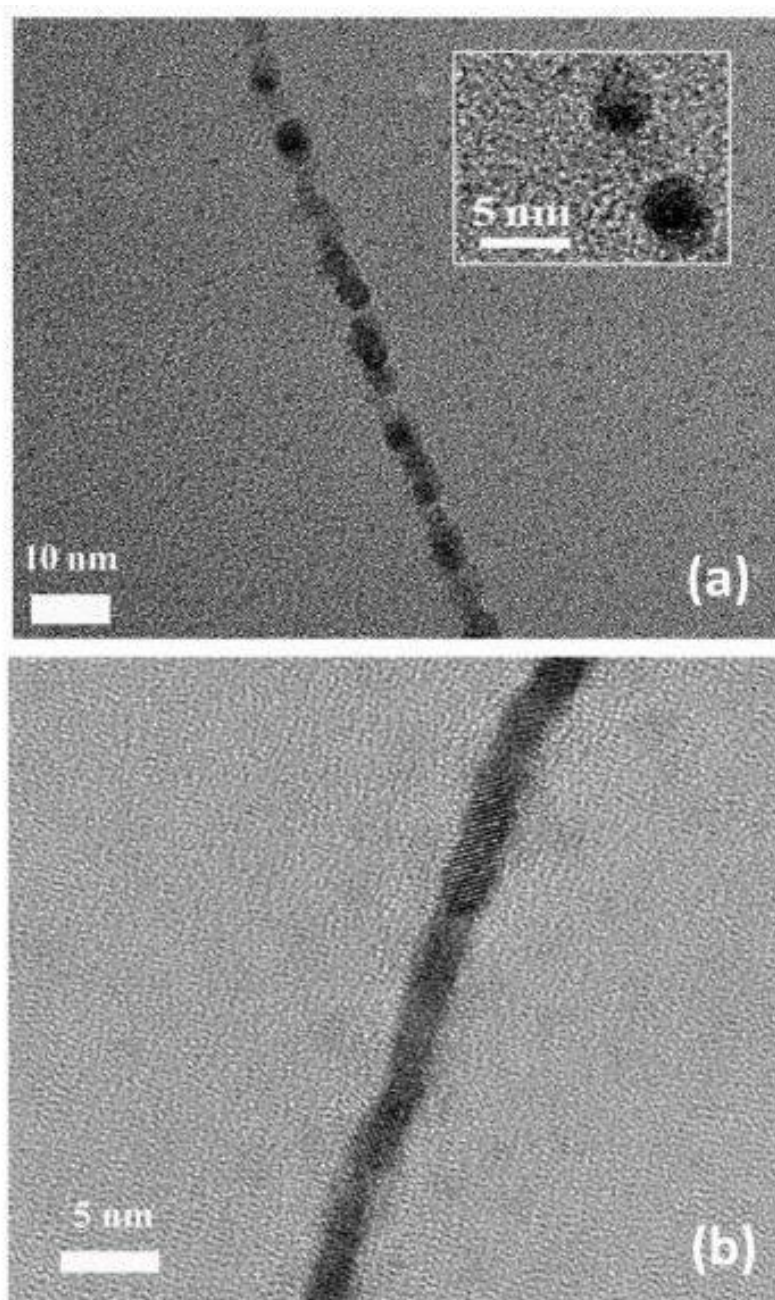

Figure 2. Cross-sectional transmission electron microscope image of the nanocrystals annealed at 900 ^{o}C for 60 s.

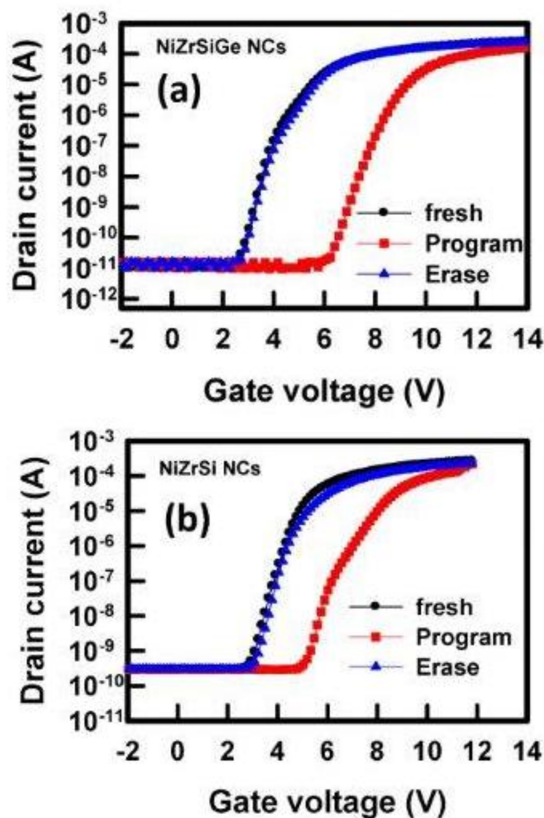

Figure 3. I_d-V_g curves of the quaternary NiZrSiGe NC memory in fresh, program, and erase states.

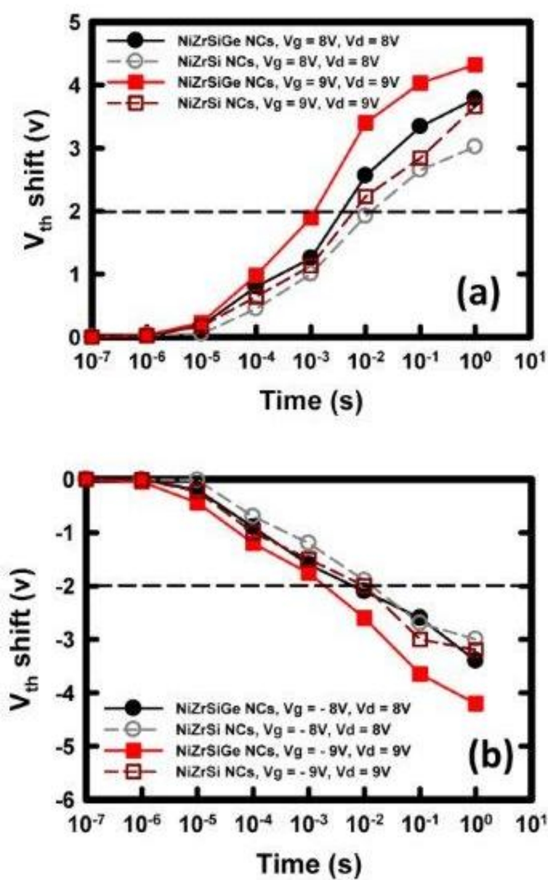

Figure 4. (a) Program and (b) erase speeds of the NC memory under different operating conditions.

Figs. 3 show the I_d-V_g curves of the quaternary NiZrSiGe and ternary NiZrSi memories in fresh, program, and erase states. A channel hot-electron injection (CHEI) mechanism was used to program the device, and a band-to-band hot-hole (BBHH) mechanism was used to erase charges in the memory devices [24]. The applied program conditions were V_g=9 V and V_d=9 V, and the erase conditions were V_g=-9 V and V_d=9 V with a 10-ms operation time. The memory window, which represents the threshold voltage (V_{th}) difference between the program and eras states, was approximately 3.84 and 2.24 V for NiZrSiGe and NiZrSi memories, respectively. The large memory window of NiZrSiGe memory is caused by more trapping site formation in the NCs. In addition, the IV curve can completely shifts back to the original fresh status after erasing. This observation is essential for a memory device to achieve greater stability and better data retention characteristics.

Figs. 4 (a) and 4(b) show the program and erase speeds, respectively, of the NiZrSiGe and NiZrSi memories under various operating conditions. The CHEI method was used to program the devices with (i) V_g=8 V, V_d=8 V and (ii) V_g=9 V, V_d=9 V. As these figures show, the V_{th} shift increases with increasing the applied program voltage, which is caused by more implantation of hot electrons into the trapping layer and are trapped in the NCs. [25]. From Fig. 4(a), the program speed can reach down to 1.1 and 6 ms for the NiZrSiGe and NiZrSi memories, respectively, for a 2 V V_{th} shift under program condition (ii) operation. Compare to the NiZrSi memory, the NiZrSiGe memory exhibits better program speed. Fig. 4(b) shows that the BBHH method was used for erase at different operating conditions: (i) V_g= -8 V, V_d= 8 V and (ii) V_g= -9 V, V_d= 9 V. The erase speed increases as the gate voltage becomes more negative. The erase speed is measured down to 2 and 10 ms for the NiZrSiGe and NiZrSi memories, respectively, for a -2 V V_{th} shift under erase condition (ii) operation.

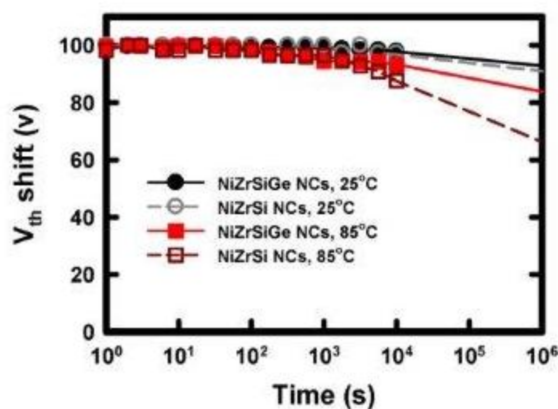

Figure 5. Charge retention characteristic of the quaternary NiZrSiGe NC memory.

This study also presented the retention and endurance characteristics of the memories to determine their reliabilities. Fig. 5 shows the charge retention characteristic of the NiZrSi and NiZrSiGe memories measured at 25 °C and 85 °C. The curves are obtained under program condition of V_g = 9V and V_d = 9V for 10 ms at 85 °C and 125 °C, respectively. For the NiZrSiGe sample measured at 25 °C, the retention time of the NiZrSiGe memory could be extrapolated up to 10^6 s with an approximate 8% charge loss, and an approximate 16% charge loss at 85 °C measurement. The

NiZrSi control sample retains the same level with NiZrSiGe memory at 25 °C, whereas much deterioration down to 34% charge loss at 85 °C measurement. This result indicates that, comparing to the NiZrSi film, the quaternary NiZrSiGe NCs serving as the charge trapping material "catch" the electrons more efficiently, even at a high temperature and long duration time.

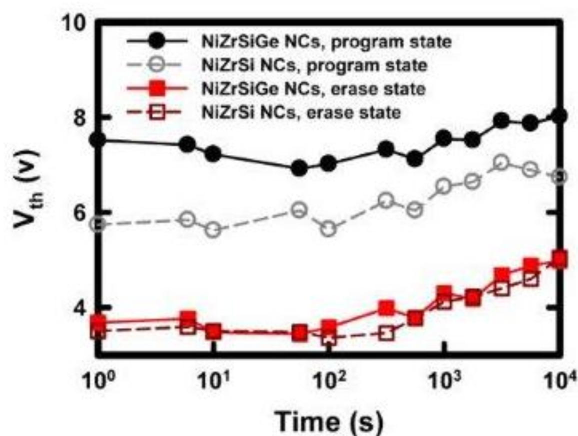

Figure 6. Endurance characteristic of the quaternary NiZrSiGe NC memory.

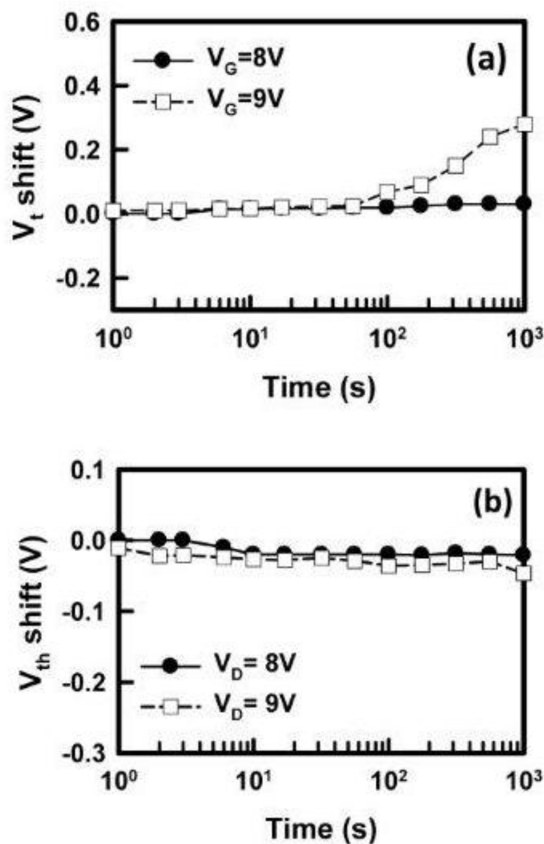

Figure 7. (a) Gate disturbance and (b) drain disturbance characteristics of the quaternary NiZrSiGe NC memories.

Fig. 6 shows the endurance characteristic of the memories at 10^4 program/erase cycles. The measured condition for programming is: V_g = 9 V, V_d = 9 V, 10 ms, and erasing is: V_g = −9V, V_d = 9V, 10 ms. The threshold-voltage shift upward is mainly caused by the interface trap generation and electron trapping in the tunneling oxide of the memories. The memory window narrowing after 10^4 P/E cycles are calculated to be 20.8 and 24.1 % for NiZrSiGe and NiZrSi memories, respectively. Compared to other sol-gel derived memories that reported previously [8-9, 17-18, 22-23], the reliabilities of the NiZrSiGe memories proposed in this study exhibits average but still acceptable performance, even though the structure and operation conditions are a little different for each memory.

In practical, the memories should be designed in array, and hence resistance to disturbance of the memory from surrounding devices needs to be examined. Therefore, quaternary NiZrSiGe NC memories are measured to address concerns regarding the gate and drain disturbances, which in turn affect device reliability. Fig. 7(a) shows the gate disturbance characteristic of the NiZrSiGe NC memory. The memory device was measured in the erase state by applying gate stresses of 8 V and 9 V. The V_{th} shift remained constant after stressing at 8 V for 10^3 s, and shifted by only 0.3 V for the 9-V gate-stressing condition. Fig. 7(b) shows the drain disturbance characteristics of the NiZrSiGe NC memory. The memory device was measured in the erase state by applying drain stresses of 8 V and 9 V, respectively. After 10^3 s of stressing, the V_{th} shift was only 0.05 V for both stressing conditions. The disturbance properties of the NiZrSiGe memories are improved comparing to other sol-gel derived memories [17-18].

4. CONCLUSION

This paper reports the fabrication of quaternary NiZrSiGe NCs to be used as the charge trapping material of flash memory by using the sol-gel spin coating method. TEM image analysis was used to confirm the crystal size and formation of nano-composite NiZrSiGe NCs. This study also investigated the electrical performance of the quaternary NiZrSiGe memories regarding the memory window, program and erase speeds, reliability, and gate and drain disturbances. Comparing to the ternary NiZrSi memory, the results demonstrate that quaternary NiZrSiGe NC memory devices exhibit improved memory performance and have the potential to be applied to advanced memory devices.

ACKNOWLEDGEMENTS
The authors would like to thank Taipei Medical University –Taipei Medical University Hospital, and Ministry of Science and Technology, for financially supporting this research under contract nos. 102TMU-TMUH-10 and NSC 102-2622-E-038-004-CC3.In addition, the authors are grateful to the National Nano Device Laboratories for their support in the fabrication process.

References

1. J. S. Oh, S. D. Yang, S. Y. Lee, Y. S. Kim, M. H. Kang, S. K. Lim, H. D. Lee, and G. W. Lee, *Microelec Eng* 103 (2013) 33.
2 C. M. Compagnoni, G. M. Paolucci, C. Miccoli, A. S. Spinelli, A. L. Lacaita, A. Visconti, and A.

Goda, *IEEE Electr Device L* 36 (2015) 132.
3 S.-H. Liu, W.-L. Yang, C.-C. Wu, and T.-S. Chao, *IEEE Electr Device L* 33 (2012) 1393.
4 Y. H. Lin, Y. C. Wu, M. F. Hung, and J. H. Chen, *Int J Electrochem Sci* 7 (2012) 8648.
5 M. K. Dai, T. Y. Lin, M. H. Yang, C. K. Lee, C. C. Huang, and Y. F. Chen, *J Mater Chem C* 2 (2014) 5342.
6 R. G. Huang and J. R. Heath, *Small* 8 (2012) 3417.
7 P. K. Singh, G. Bisht, K. Auluck, M. Sivatheja, R. Hofmann, K. K. Singh, and S. Mahapatra, *IEEE T Electron Dev* 57 (2010) 1829.
8 C.-C. Wu, F.-H. Ko, W.-L. Yang, H.-C. You, F.-K. Liu, C.-C. Yeh, P.-L. Liu, C.-K. Tung, and C.-H. Cheng, *IEEE Electr Device L* 31 (2010) 746.
9 C.-C. Wu, Y.-J. Tsai, M.-C. Chu, S.-M. Yang, F.-H. Ko, P.-L. Liu, W.-L. Yang, and H.-C. You, *Appl Phy Lett* 92 (2008) 123111.
10 A. Das, S. Maikap, C. H. Lin, P. J. Tzeng, T. C. Tien, T. Y. Wang, L. B. Chang, J. R. Yang, and M. J. Tsai, *Microelec Eng* 87 (2010) 1821.
11 T. H. Ng, W. K. Chim, W. K. Choi, V. Ho, L. W. Teo, A. Y. Du, and C. H. Tung, *Appl Phy Lett* 84 (2004) 4385.
12 A. M. Hartel, S. Gutsch, D. Hiller, C. Kubel, N. Zakharov, P. Werner, and M. Zacharias, *Appl Phy Lett* 101 (2012).
13 B. Li and J. L. Liu, *IEEE transactions on nanotechnology* 10 (2011) 284.
14 S. Choi, S. S. Kim, H. Yang, M. Chang, S. Jeon, C. Kim, D. Y. Kim, and H. Hwang, *Microelec Eng* 80 (2005) 264.
15 H. S. Kim, D. W. Kim, S. Ahn, Y. C. Kim, J. Cho, S. K. Choi, and D. Y. Kim, *Microelec Eng* 78-79 (2005) 55.
16 C. W. Hu, T. C. Chang, P. T. Liu, C. H. Tu, S. K. Lee, S. M. Sze, C. Y. Chang, B. S. Chiou, and T. Y. Tseng, *Appl Phy Lett* 92 (2008).
17 H.-C. You, C.-C. Wu, F.-H. Ko, T.-F. Lei, and W.-L. Yang, *J Vac Sci Technol B* 25 (2007) 2568.
18 C.-C. Wu, Y.-J. Tsai, P.-L. Liu, W.-L. Yang, and F.-H. Ko, *J Mater Sci: Mater Elec* 24 (2012) 423.
19 B. B. Yu, C. A. Turdean-Ionescu, R. A. Martin, R. J. Newport, J. V. Hanna, M. E. Smith, and J. R. Jones, *Langmuir* 28 (2012) 17465.
20 H. P. Xiang, J. F. Ge, S. H. Cheng, H. M. Han, and S. W. Cui, *J Sol-Gel Sci Techn* 59 (2011) 635.
21 C. C. Liu, Z. F. Liu, J. W. Li, Y. B. Li, J. H. Han, Y. Wang, Z. C. Liu, and J. Ya, *Microelec Eng* 103 (2013) 12.
22 C.-C. Wu, W.-L. Yang, Y.-M. Chang, S.-H. Liu, and Y.-P. Hsiao, *Int J Electrochem Sci* 8 (2013) 6678.
23 F. H. Ko, H. C. You, C. M. Chang, W. L. Yang, and T. F. Lei, *J Electrochem Soc* 154 (2007) H268.
24 Y. Tsuji, M. Terai, S. Fujieda, T. Syo, T. Saito, and K. Ando, *IEEE T Electron Dev* 57 (2010) 466.
25 Y. H. Lin, H. C. You, and C. H. Chien, *J Vac Sci Technol B* 30 (2012).

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